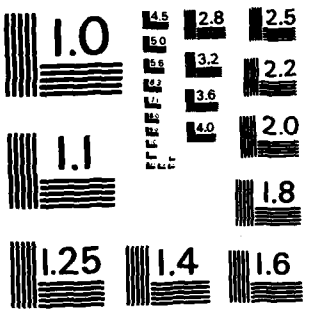
AD-A139 570 SYNCHRONISATION TECHNIQUE OF DATA RECORDED ON A MULTICHANNEL TAPE RECORDER(U) ENGINEERING DEVELOPMENT ESTABLISHMENT MARIBYRNONG (AUSTRALIA) J D DICKENS 1/1

UNCLASSIFIED JAN 84 EDE-1/84 F/G 14/3 NL



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS - 1963 - A

AR-002-713

(12)

AD A139570

AUSTRALIAN ARMY

ENGINEERING DEVELOPMENT ESTABLISHMENT

SYNCHRONISATION TECHNIQUE OF DATA RECORDED ON A MULTICHANNEL TAPE RECORDER

BY

J.D. DICKENS

© Commonwealth of Australia

THIS UNITED STATES NATIONAL TECHNICAL INFORMATION SERVICE IS AUTHORISED TO REPRODUCE AND SELL THIS REPORT

DTIC
ELECTE
MAR 30 1984
A

APPROVED

FOR PUBLIC RELEASE

DTIC FILE COPY

84 03 29 100

AUSTRALIAN ARMY

ENGINEERING DEVELOPMENT ESTABLISHMENT

SYNCHRONISATION TECHNIQUE OF DATA RECORDED ON A MULTICHANNEL TAPE RECORDER

BY

J.D. DICKENS

DTIC ELECTE MAR 30 1984 S D

PUBLICATION EDE 1/84

Prepared and issued under my direction.

(P.J.A.Evans)
Brigadier
Commander

MARIBYRNONG VICTORIA

PRIVATE BAG 12,
P O ASCOT VALE,
VICTORIA 3032.

© COMMONWEALTH OF AUSTRALIA 1984

Approved for Public Release

Distribution

Addressee	No of Copies
Army Office	
CMAT	1
DGMAT	1
DGAQA	1
HQ Log Comd	
P&E Group	1
Defence Science and Technology Organisation	
CDS for DCDS, CPAS, SSTP	1
DISB, (Document Exchange Centre)	18
DTRIALS	1
Scientific Adviser (Navy)	1
(Army)	1
(Air Force)	1
Superintendent CSE	1
ARL Library	1
DRCS Library	1
MRL Library	1
VIC D	1
DCL (CP)	1
Counsellor, Defence Science, Washington	*
Defence Science Representative London	*
* Document Control Data Sheet only	
Internal	
COMD	1
SEE	1
SME	1
SEF	1
DIL	1
S&P	1
Library	2
Author	1
File	1
Spare	7
Total	50

Accession For
NTIS GRA&I ☒
DTIC TAB ☐
Unannounced ☐
Justification
By
Distribution/
Availability Codes
Dist | Avail and/or Special
A-1

Publication EDE 1/84

ENGINEERING DEVELOPMENT ESTABLISHMENT

SYNCHRONISATION TECHNIQUE OF DATA RECORDED ON A MULTICHANNEL TAPE RECORDER

SUMMARY

This document describes the design and development of

A portable, self-contained, electronic digital unit, termed Data Synchroniser, was designed and developed. This unit is able to time synchronise recorded data channels from a multi-channel tape recorder during playbacks. During the data recording, it produces a synchronisation signal which is recorded on one channel using direct or FM techniques. The recording/playback speed ratio may be varied to suit the analysis method. Patent applications are pending.

frequency modulation.

Maribyrnong
January 1984 PUBLICATION EDE 1/84

ENGINEERING DEVELOPMENT ESTABLISHMENT

SYNCHRONISATION TECHNIQUE OF DATA RECORDED ON A MULTICHANNEL TAPE RECORDER

BY

J.D. DICKENS

INTRODUCTION

1. The problem existed of time synchronising, during playback, of three accelerometer signals recorded on a seven channel FM magnetic tape recorder. This occurred because the recorded data was to be analysed by a digital computer system, with only two input channels. Furthermore, it was necessary to leave the instrumentation unattended during recording, because the physical phenomena being investigated was of short duration (about half a second) and its time of occurrence was unknown (magnetic tapes had to be replaced every three hours).

REQUIREMENT

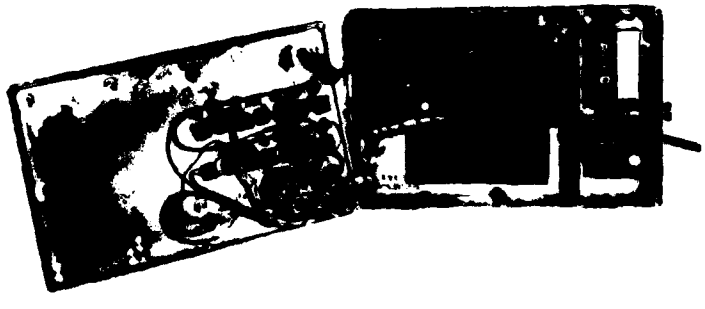
2. To produce a unit capable of synchronising recorded data during playback of an Ampex FM tape recorder type FR 1300 into a Hewlett Packard digital computer system type 2100S/5451B.

DISCUSSION

3. A unit, called a Data Synchroniser (DS), conforming to the requirement of this Report, was designed, constructed, tested and used. It requires an external 240 V, 50 Hz single phase AC power supply, and a signal generator during recording. It is depicted in Figs 1 and 2.

7748A

FIG 1 EXTERNAL VIEW OF DATA SYNCHRONISER



7748B

FIG 2 INTERNAL VIEW OF DATA SYNCHRONISER

OPERATION

Recording Mode

4. A block diagram of the recording system is shown in Fig 3.

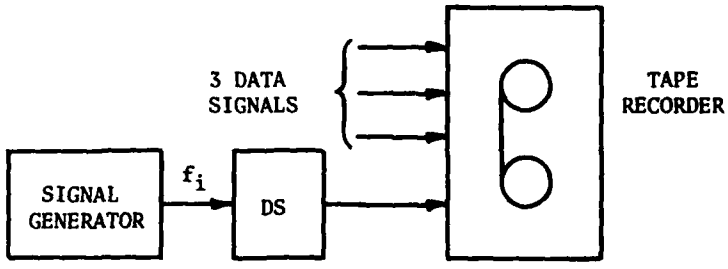


FIG 3 RECORDING SYSTEM

5. The DS provides a three level digital signal for recording having voltage levels -1V, 0V and 1V. The frequency of this signal, f_i, is set from a signal generator and is determined from the desired delay resolution and the recording characteristics of the tape recorder. This signal requires one data channel and may be recorded using direct or FM techniques.

Playback Mode

6. A block diagram of the playback system is shown in Fig 4.

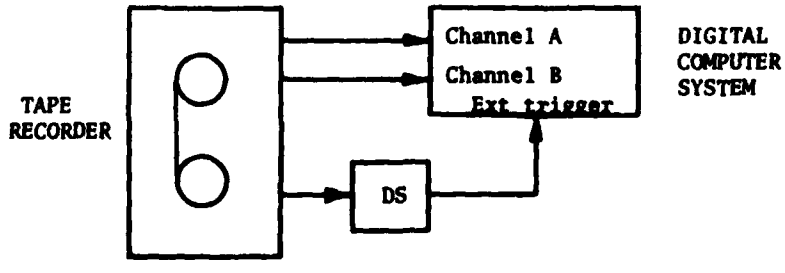


FIG 4 PLAYBACK SYSTEM

7. The DS decodes the recorded three level digital signal during playback and provides an output synchronising pulse to externally trigger the computer system. This pulse occurs at the same instant relative to the data recorded each time the tape is played back, regardless of the playback speed.

8. The synchronising pulse may be delayed time-wise in steps of $\Delta t'$, given by

$$\Delta t' = \frac{\text{Tape recording speed}}{\text{Tape playback speed}} \times \frac{1}{2f_i}$$

The required delay is easily determined by using the HOLD facility of the DS.

9. The pulse is TTL compatible and allows for easy interfacing with TTL compatible circuits, and for positive and negative edge triggering.

10. Using this technique, two data channels are stored in the digital computer system, and then the process is repeated to store the third data channel, thus maintaining time fidelity between the signals. Obviously this technique can be extended to include all unused channels of the tape recorder.

CIRCUIT DESCRIPTION (Diagrams at Annex A)

11. Circuit diagrams of the DS are shown in Figs 1 and 2. A block diagram of the data processor is shown in Fig 3 and a timing diagram in Fig 4.

Record Mode

12. Refer to Figs 1, 2, 3 and 4.

13. The required switch positions are as follows:

SW 1: ON

SW 3: COUNT

SW 4: RECORD

SW 5: OUT

SW 18: desired SEQUENCE LENGTH, N

Other switches: any position

14. A signal generator is used to feed a square wave of freqency f_i and voltage levels 0, 1V into the record input connector J1. The unity gain buffer 3A presents this input signal to comparator 4B. The output from 4B is inverted and converted to TTL levels by transistor Q1. The Q output of the latch 6B follows its data input D, and drives the binary counter 7 which gives ÷2, ÷4, ÷8 and ÷16 outputs. The ÷16 output drives the binary counter 8 which gives ÷32, ÷64, ÷128 and ÷256 outputs. The ÷256 output drives the binary counter 9 which gives ÷512, ÷1024, ÷2048 and ÷4096 outputs.

15. All of these outputs from the three binary counters and the output from latch 6B are inverted by buffers 10A to 10F, 11A to 11F and 15B. These buffered outputs drive indicators I2 to I14 which show the state of the counters.

16. Switches SW 5 to SW 17 determine which signals are fed into the NAND gates 12A, 12B, 13A and 13B. These NAND gates and the inverters 14A to 14D are equivalent to a 13-input AND gate, whose nett effect is to produce a pulse at the output of 14D once every time T, as determined by switch SW 18. This output is subtracted from the output of Q1, by amplifier 3B, and the resulting signal is made available for recording at connector J2.

17. Every time 14D pulses. monostable 5B is triggered and lights up indicator I16 for about 0.25 seconds via buffer 15C.

Playback Mode

18. Refer to Figs 1, 2, 3 and 4.

19. The required switch positions are as follows:

SW 1: ON

SW 2: INHIBIT resets counters unless SW 3 in HOLD
ENABLE allows counting to commence when negative pulse appears at J1

SW 3: COUNT allows counting
HOLD stops counting and holds counted value

SW 4: PLAYBACK

SW 5 - SW 17: desired DELAY

SW 18: $\geq N$

20. The recorded synchronising waveform is played back into connector J1. This is a three level digital signal with voltage levels -1V, 0V and 1V. The unity gain buffer 3A presents this signal to comparator 4A, which produces a positive pulse output every time a negative pulse occurs at J1. This happens at intervals of time T'.

21. The output from 4A is inverted and converted to TTL levels by transistor Q2, which controls the triggering of monostable 5A. The latch 6A is triggered by negative going edges and hence produces an output pulse every time the leading edge of a negative pulse appears at J1. The monostable may be inhibited by switch SW 2, which consequently controls which negative pulse at J1 produces a monostable pulse. This pulse is high for about 70 seconds, which after being inverted by buffer 15A enables the binary counters 7, 8 and 9 to count. This counting mode is indicated by indicator I16.

22. Enabling the latch 6A during a monostable pulse ensures that the binary counters are not reset, which would otherwise happen at the end of the pulse.

23. Because switch SW 3 enables latches 6A and 6B, at any instant it may be used to stop the counting and indicate the count value by means of indicators I2 and I14. Hence during the preliminary playback, SW 3 is put into HOLD at the required instant and then SW 5 to SW 17 are placed in the ON position if the corresponding indicators are lit. This playback may be done at a slow speed to make the process easier. Desirable small changes in the delay may be determined experimentally.

24. Switch SW 2 is put into ENABLE anytime between the negative pulse at J1 which is required to start the counting, and the previous negative pulse. Putting it into INHIBIT immediately resets the binary counters, provided that SW 3 is in the COUNT position.

25. The rest of the circuit operates as described under RECORD MODE, which produces an output pulse at connector J3 after the desired delay as determined by switches SW 5 to SW 17.

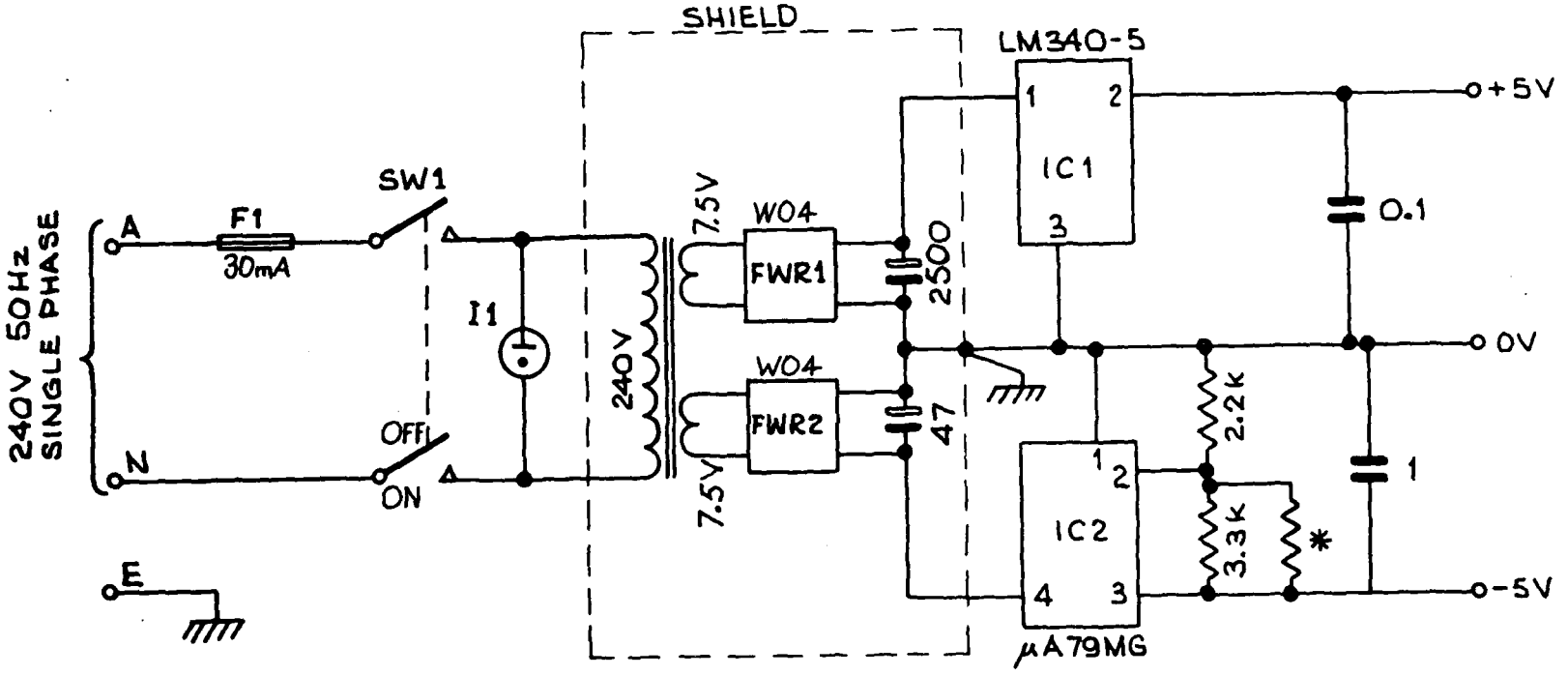
APPLICATION

26. Typical parameter values for this application were as follows:

Tape recording speed	= 95.25 mm/s
f_i	= 40 Hz
Δt	= 12.5 ms
N	= 1024
T	= 12.8 s
Tape playback speed	= 92.25 mm/s
$\Delta t'$	= 12.5 ms

CONCLUSION

27. The Data Synchroniser described satisfied the requirement to synchronise recorded data channels from a multi-channel tape recorder during playback. It requires only one data channel, which may be recorded using direct or FM techniques, is simple to operate and any recording/playback speed ratio may be used.



NOTES RESISTANCE VALUES IN Ω
CAPACITANCE VALUES IN μF

* SET ON TEST

FIG 1 POWER SUPPLY - CIRCUIT DIAGRAM

ANNEX A

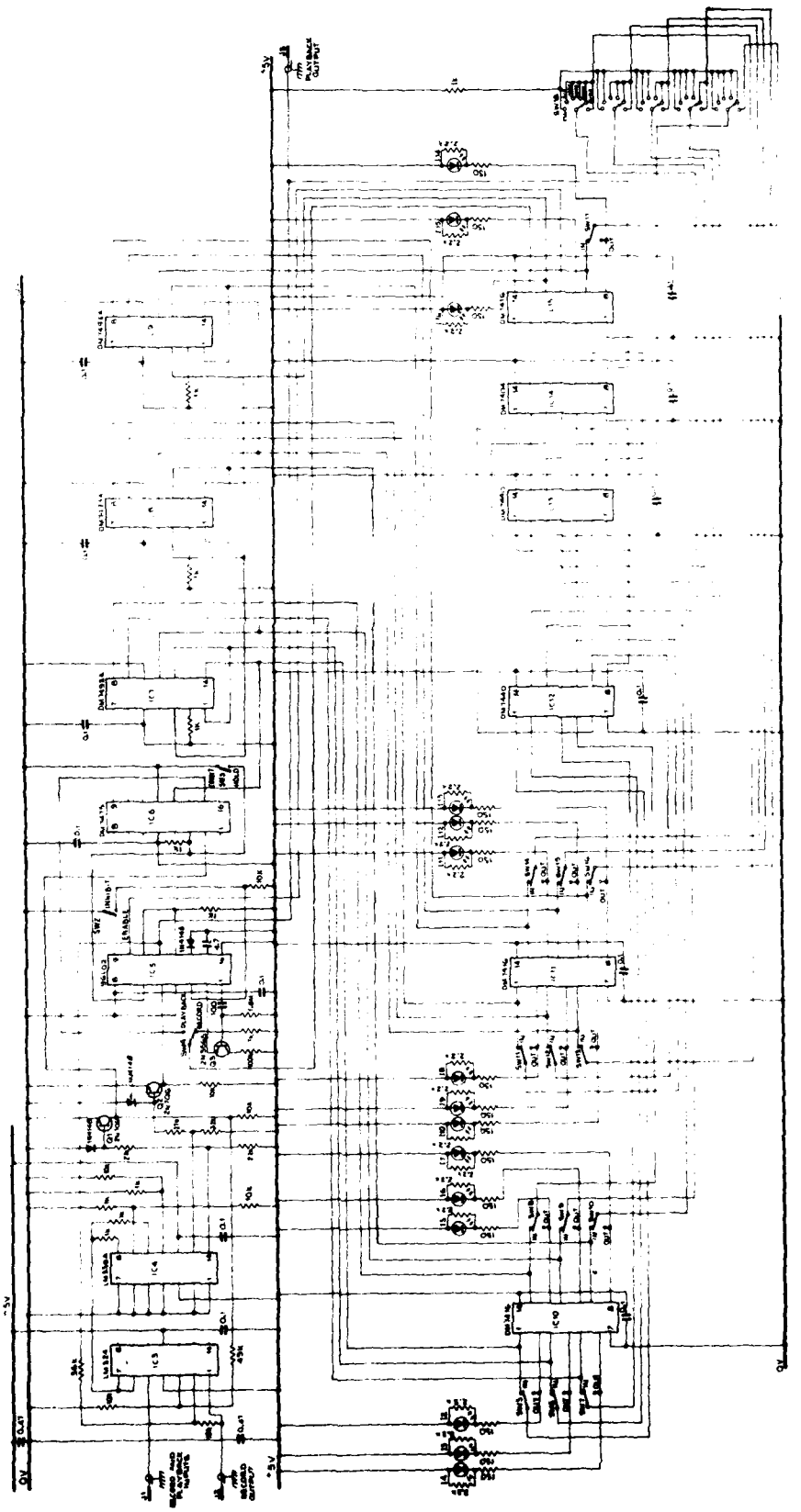


FIG 2 DATA PROCESSOR - CIRCUIT DIAGRAM

ANNEX A

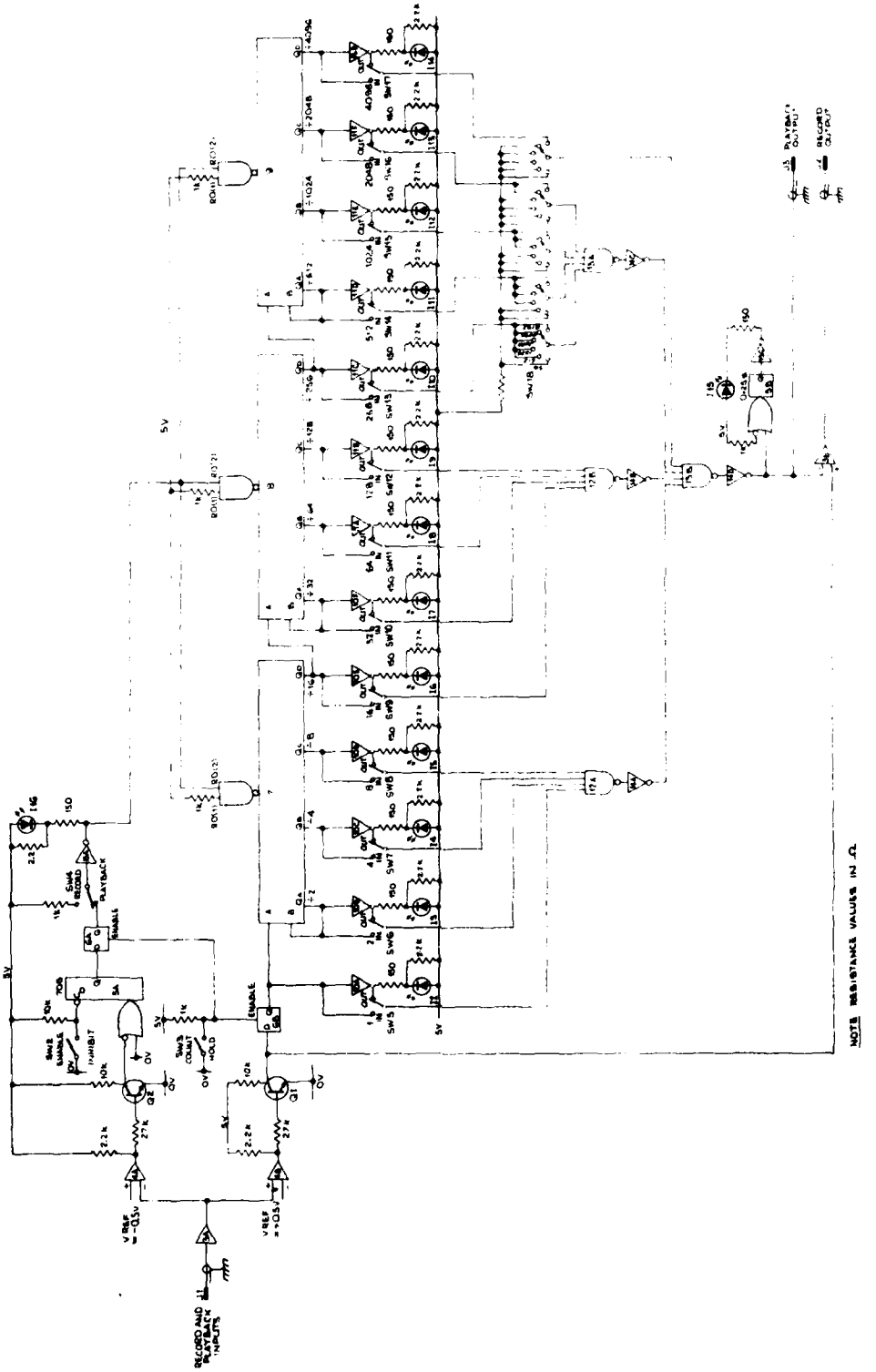
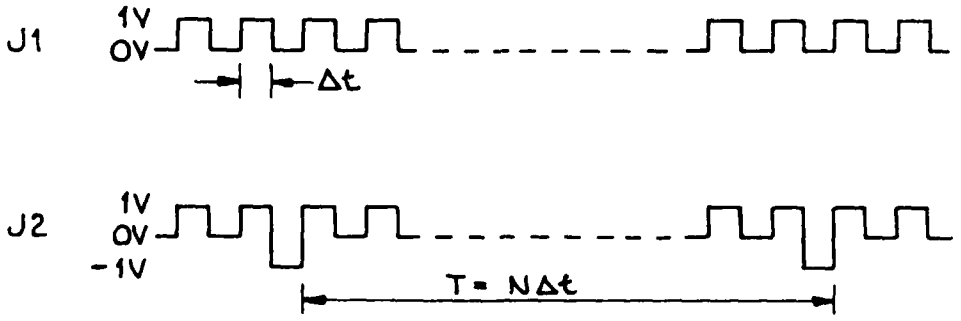
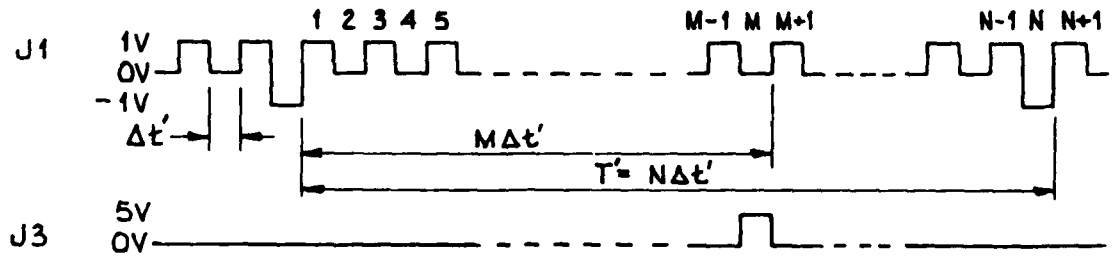


FIG 3 DATA PROCESSOR - BLOCK DIAGRAM

RECORD MODE



PLAYBACK MODE



NOTE

N = SEQUENCE LENGTH

$\Delta t = \frac{1}{2f_i}$ WHERE f_i = RECORDING FREQUENCY

$$\Delta t' = \frac{\text{TAPE RECORDING SPEED}}{\text{TAPE PLAYBACK SPEED}} \Delta t$$

$$M = \sum_{n=0}^{12} C_n 2^n \quad \text{WHERE} \quad C_n = \begin{cases} 0 \text{ IF SWITCH } 2^n \text{ IN "OUT" POSITION.} \\ 1 \text{ IF SWITCH } 2^n \text{ IN "IN" POSITION} \end{cases}$$

FIG 4 TIMING DIAGRAM

DOCUMENT CONTROL DATA

1.a. AR No	1.b. Establishment No	2. Document Date	3. Task No
002-713	EDE 1/84	January 1984	DST 79/226

4. Title	5. Security	6. No Pages
Synchronisation Technique of Data Recorded on a Multichannel Tape Recorder	a. document U b. title U c. abstract U	10 7. No Refs

8. Author(s)	9. Downgrading Instructions
J.D. Dickens	NA

10. Corporate Author and Address	11. Authority (as appropriate)
Engineering Development Establishment Maribyrnong Victoria	a. Sponsor c. Downgrading b. Security d. Approval NA

12. Secondary Distribution (of this document)

Approved for Public Release

13.a. This document may be ANNOUNCED in catalogues and awareness services available to...

No Limitation

14. Descriptors	15. COSATI Group
Data recording Magnetic recording Data retrieval Synchronizers	

16. Abstract

A portable, self-contained, electronic digital unit, termed Data Synchroniser was designed and developed by EDE. This is able to synchronise recorded data channels from a multichannel tape recorder during playback. During the data recording it produces a synchronisation signal which is recorded on one channel using either direct or FM techniques. The recording/playback speed ratio may be varied to suit the analysis method. Patent applications are pending.

8324

END

DATE
FILMED

4 84

DTIC